Claim Amendment

Please amend claims 1, 3, 5, and 12 as follows.
Please cancel claims 4 and 13.
Please add new claim 21 as follows.

1. (currently amended) A semiconductor wafer dry etching system comprising:

a plasma chamber ~~in which at least polymerizing gas is introduced, excess polymer forming and subsequently peeling off inner vertical walls of the chamber and falling down due to gravity; and,~~;

a ~~electrically biased mechanism~~ vertically moveable wafer lifter to hold a semiconductor wafer in a face down processing position during plasma processing at a top of the plasma chamber, the semiconductor wafer and the wafer lifter supplied with an electrical bias during plasma processing; ~~such that the polymer is electrostatically attracted to the wafer, positioning of the wafer at the top of the chamber preventing the excess polymer from falling onto the wafer,~~ the ~~electrically biased mechanism~~ semiconductor wafer lifter comprising:

~~a wafer lifter positioned at the top of the plasma chamber, having~~ wherein the wafer lifter further comprises sidewalls defining a first diameter greater than a diameter of the semiconductor wafer and a bottom portion having a ~~hole~~ circular

opening therein, said circular opening having a second diameter less than the first diameter and less than the diameter of the semiconductor wafer, ~~the wafer exposed from the bottom of the wafer lifter through the hole therein,~~; and,

wherein the semiconductor wafer periphery rests on an inner top surface of the bottom portion defining the circular opening to expose the semiconductor wafer processing face during plasma processing ~~of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter both completely perpendicular as a whole to the sidewalls of the wafer lifter defining the first diameter greater than the diameter of the wafer~~.

2. (cancelled)

3. (currently amended) The system of claim 1, wherein the ~~electrically biased mechanism further comprises~~ electrical bias is supplied through a wafer chuck in contact with the semiconductor wafer and the wafer lifter.

4. (cancelled)

5. (currently amended) The system of claim 1 [[4]], wherein the wafer lifter is vertically movable between a lower wafer loading position to the face down processing position ~~between a lower position to an upper position, where the lower position promotes loading of the wafer to the wafer lifter, and the upper position enables the bias supply to electrically couple with the wafer chuck for biasing of the wafer~~.

6. (cancelled)

7. (original) The system of claim 1, further comprising one or more coils to induce a varying magnetic field within the chamber.

8. (original) The system of claim 7, wherein the one or more coils comprise one or more induction coils.

9. (original) The system of claim 7, wherein the one or more coils comprise one or more electromagnetic coils.

10. (original) The system of claim 7, further comprising one or more multi-pole magnets cooperating with the one or more coils to assist inducement of the varying magnetic field within the chamber.

11. (original) The system of claim 1, further comprising a dielectric window at a bottom of the chamber.

12. (currently amended) A semiconductor wafer dry etching system comprising:

a plasma chamber ~~in which at least polymerizing gas is introduced~~;

a wafer lifter to hold a semiconductor wafer ~~upside down~~ exposing a face down processing surface at a top of the plasma chamber during plasma processing, the wafer lifter ~~positioned at the top of the plasma chamber,~~ having sidewalls defining a first diameter greater than a diameter of the wafer and a bottom portion having a hole therein having a second diameter less than the first diameter and less than the diameter of the wafer[[,]]; wherein the wafer periphery is positioned on an inner top surface of the bottom portion to expose the face down processing surface ~~exposed from the bottom of the wafer lifter~~ through the hole therein; and,

a bias supply to bias ~~the~~ a wafer chuck contacting the backside of the wafer and contacting the wafer lifter during plasma processing and ~~the wafer, such that polymer is electrostatically attracted to the wafer,~~

~~wherein the wafer rests on an inner top surface of the bottom of the wafer lifter that is completely parallel as a whole to an outer bottom surface of the bottom of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter completely perpendicular as a whole to the sidewalls of the wafer lifter defining the first diameter greater than the diameter of the wafer~~.

13. - 14. (cancelled)

15. (original) The system of claim 12, wherein the wafer lifter is vertically movable between a lower position to an upper position, where the lower position promotes loading of the wafer, and the upper position enables the bias supply to electrically couple with the wafer for biasing thereof.

16. (original) The system of claim 12, further comprising one or more coils to induce a varying magnetic field within the chamber.

17. (original) The system of claim 16, wherein the one or more coils comprise one or more induction coils coupled.

18. (original) The system of claim 16, further comprising one or more magnets cooperating with the one or more coils to assist inducement of the varying magnetic field within the chamber.

19. (original) The system of claim 12, further comprising a dielectric window at a bottom of the chamber.

20. (withdrawn) A method comprising:

lowering a wafer lifter positioned over a plasma chamber of a semiconductor dry etching system;

loading a semiconductor wafer upside-down into the wafer lifter;

raising the wafer lifter to electrically couple the wafer with a cathode of the semiconductor dry etching system; and,

performing dry etching semiconductor processing on the wafer.

21. (new) The system of claim 12, wherein the inner top surface of the bottom portion of the wafer lifter is substantially parallel to an outer bottom surface of the bottom portion of the wafer lifter, the inner top surface and the outer bottom surface of the bottom of the wafer lifter substantially perpendicular to the sidewalls of the wafer lifter defining the first diameter greater than the diameter of the wafer.